What is claimed is:

1. A semiconductor protection element comprising:

a semiconductor substrate having a first region of a first impurity concentration and a pair of second regions having a second impurity concentration being higher than that of said first region; and

silicide layers each being formed in a manner so as to be in contact with a surface of each of said second regions;

wherein said first region has a first surface region not covered with said silicide layers and said second regions have second surface regions not covered with said silicide layers and said first surface region is sandwiched by two said second surface regions;

wherein each of said silicide layers is formed in a manner that each of said second surface regions is in contact with said first surface region in a continued manner and that each of said second surface regions is exposed; and

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second surface regions makes up an intermediate resistance region having an intermediate resistance value, and said first surface region makes up a high resistance region having a relatively high resistance value.

2. The semiconductor protection element according to Claim 1, wherein a field oxide film is formed on said first surface region or on said first exposed region.

3. The semiconductor protection element according to Claim 1, wherein a gate electrode structure is formed on said first surface region or on said first exposed region.

4. A semiconductor protection element comprising:

a semiconductor substrate having a first region of a first impurity concentration and a pair of second regions having a second impurity concentration being higher than that of said first region; and

silicide layers each being partially formed in a manner so as to be in contact with a surface of said second regions;

wherein said first region has a first exposed region being exposed on a surface of said semiconductor substrate and each of said silicide layers is so formed as to have a second exposed region in which part of each of said second regions is exposed on a surface of said semiconductor substrate in a manner so as to continuously be in contact with said first exposed region;

wherein said first exposed region is sandwiched by two said second regions; and

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second region makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said first region makes up a high resistance region having a relatively high resistance value.

5. The semiconductor protection element according to Claim 4, wherein said first region is made up of a well region.

6. The semiconductor protection element according to Claim 4, wherein said first region is formed on a surface of said semiconductor substrate and in a manner that said first region and said second region are overlapped on a surface of said semiconductor substrate.

7. The semiconductor protection element according to Claim 6, wherein, said first impurity concentration of said first region, when it is assumed that a well region is formed on said semiconductor substrate, is higher than that of said well region.

8. The semiconductor protection element according to Claim 4, wherein a field oxide film is formed on said first surface region or on said first exposed region.

9. The semiconductor protection element according to Claim 4, wherein a gate electrode structure is formed on said first surface region or on said first exposed region.

10. The semiconductor protection element according to Claim 4, wherein said second exposed region has a surface length being equal to or larger than that of said first exposed region.

11. The semiconductor protection element according to Claim 4, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

12. A semiconductor protection element comprising:

a semiconductor substrate having a first region of a first impurity concentration and a pair of second regions having a second impurity concentration being higher than that of said first region;

wherein said first region is made up of a well region;

wherein, on said first region, a third region of a third impurity concentration being higher than said first impurity concentration and being lower than said second impurity concentration is formed;

wherein said third region is sandwiched by two said second regions, makes up a first exposed region being exposed on a surface of said semiconductor substrate and, on a surface of said semiconductor substrate, said third region and said second region are overlapped each other;

wherein each of said silicide layers is so formed as to have a second exposed region in which part of each of said second regions is exposed on a surface of said semiconductor substrate in a manner so as to continuously be in contact with said first exposed region; and

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second region makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said third region makes up a high resistance region having a relatively high resistance value.

13. The semiconductor protection element according to Claim 12, wherein a field oxide film is formed on said first surface region

or on said first exposed region.

14. The semiconductor protection element according to Claim 12, wherein a gate electrode structure is formed on said first surface region or on said first exposed region.

15. The semiconductor protection element according to Claim 12, wherein said second exposed region has a surface length being equal to or larger than that of said first exposed region.

16. The semiconductor protection element according to Claim 12, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

17. A method for manufacturing a semiconductor protection element comprising:

a first step of implanting an impurity into a semiconductor substrate to form a first region of a first impurity concentration;

a second step of forming a pair of second regions having a second impurity concentration being higher than said first impurity concentration on both sides of said first region on a surface of said semiconductor substrate; and

a third step of forming silicide layers being in contact with a surface of said second region;

wherein, in said third step, each of said silicide layers is formed in a manner that said first region has a first surface region not covered by said silicide layers and said second region has a second surface region not covered by said silicide layers

and that said first surface region is sandwiched by two said second surface regions; and

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second surface regions makes up an intermediate resistance region having an intermediate resistance value, and said first surface region makes up a high resistance region having a relatively high resistance value.

18. A method for manufacturing a semiconductor protection element comprising:

a first step of implanting an impurity into a semiconductor substrate to form a first region of a first impurity concentration;

a second step of forming a pair of second regions having a second impurity concentration being higher than said first impurity concentration on both sides of a first exposed region being exposed in said first region and on a surface of said semiconductor substrate; and

a step of forming each of said silicide layers being in contact with a surface of said second region so that part of each of said second regions is exposed on said surface of said semiconductor substrate succesively so as to be in contact with said first exposed region of said first region;

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second region makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said first region makes

up a high resistance region having a relatively high resistance value.

19. The method for manufacturing a semiconductor protection element according to Claim 18, wherein each of said second regions and said first region are overlapped each other on a surface of said semiconductor substrate.

20. The method for manufacturing a semiconductor protection element according to Claim 19, wherein, said first impurity concentration of said first region, when it is assumed that a well region is formed on said semiconductor substrate, is higher than that of said well region.

21. The method for manufacturing a semiconductor protection element according to Claim18, wherein said second exposed region has a surface length being equal to or larger than that of said first exposed region.

22. The method for manufacturing a semiconductor protection element according to Claim 18, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

23. A method for manufacturing a semiconductor protection element comprising:

a step of implanting an impurity into a semiconductor substrate to form a first region of a first impurity concentration;

a step of forming a third region having a third impurity concentration being higher than said first impurity concentration in a manner that said third region and said first region are overlapped on a surface of said semiconductor substrate;

a step of forming a pair of second regions having a second impurity concentration being higher than that of said third region on both sides of a first exposed region being exposed in said third region and on a surface of said semiconductor substrate;

a step of forming each of said silicide layers being in contact with a surface of said second region so that part of each of said second regions is exposed on a surface of said semiconductor substrate successively so as to be in contact with said first exposed region of said first region;

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second region makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said third region makes up a high resistance region having a relatively high resistance value.

24. The method for manufacturing a semiconductor protection element according to Claim23, wherein said second exposed region has a surface length being equal to or larger than that of said first exposed region.

25. The method for manufacturing a semiconductor protection element according to Claim 23, wherein a surface length of said second exposed region is equal to or larger than a depth of said

second region.

26. A semiconductor device comprising:

a semiconductor substrate having a first region of a first impurity concentration and a first "second region", second "second region" and third "second region" each having a second impurity concentration being higher than that of said first region;

silicide layers each being formed in a manner so as to be in contact with a surface of each of said first "second region", second "second region" and third "second region";

one of a source electrode and a drain electrode being formed on one of said silicide layers formed in a manner so as to be in contact with the surface of said first "second region";

a gate electrode constructed between said silicide layers formed in a manner so as to be in contact with the surfaces of said first "second region" and second "second region"; and

another of said source electrode and said drain electrode being formed on another out of said silicide layers formed in a manner so as to be in contact with the surface of said third "second region";

wherein said first region, said second "second region", and said third "second region" have, respectively, a first surface region, second "second surface region", and third "second surface region" all being positioned between said silicide layers formed in a manner so as to be in contact with the surfaces of said second "second region" and third "second region" and all being not covered with said silicide layers;

wherein said first surface region is formed in a manner so

as to be sandwiched between said second "second surface region" and third "second surface region";

wherein each of said silicide layers is constructed in a manner that said second "second surface region" and third "second surface region" are formed so as to be in contact with the surface of said first surface region and so as to expose said second "second surface region" and third "second surface region";

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second surface regions makes up an intermediate resistance region having an intermediate resistance value, and said first surface region makes up a high resistance region having a relatively high resistance value.

27. The semiconductor device according to Claim 26, wherein a field oxide film is formed on said first surface region or said first exposed region.

28. The semiconductor device according to Claim 26, wherein a gate electrode structure is formed on said first surface region or said first exposed region.

29. A semiconductor device comprising:

a semiconductor substrate having a first region of a first impurity concentration and a first "second region", second "second region" and third "second region" each having a second impurity concentration being higher than that of said first region;

silicide layers each being formed in a manner so as to be

in contact with a surface of each of said first "second region", second "second region" and third "second region";

one of a source electrode and a drain electrode being formed on one of the silicide layers formed in a manner so as to be in contact with the surface of said first "second region";

a gate electrode constructed between said silicide layers formed in a manner so as to be in contact with the surfaces of said first "second region" and second "second region"; and

another of said source electrode and said drain electrode being formed on another out of said silicide layers formed in a manner so as to be in contact with the surface of said third "second region";

wherein said first region has a first exposed region on a surface of said semiconductor substrate between said second "second region" and third "second region";

wherein each of said silicide layers is formed so as to have a second exposed region in a manner that said second "second region" and third "second region" are in contact with said second exposed region in a continuous manner;

wherein said first exposed region is sandwiched between said second "second region" and third "second region";

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second "second region" and third "second region"makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said first region makes up a high resistance region having a relatively high resistance value.

30. The semiconductor device according to Claim 20, wherein said first region is made up of a well region.

31. The semiconductor device according to Claim 29, wherein said first region is formed on a surface of said semiconductor substrate and said first region and said second region are overlapped each other on a surface of said semiconductor substrate.

32. The semiconductor device according to Claim 31, wherein, said first impurity concentration of said first region, when it is assumed that a well region is formed on said semiconductor substrate, is higher than that of said well region.

33. The semiconductor device according to Claim 29, wherein a field oxide film is formed on said first surface region or said first exposed region.

34. The semiconductor device according to Claim 29, wherein a gate electrode structure is formed on said first surface region or said first exposed region.

35. The semiconductor device according to Claim 29, wherein said second exposed region has a surface length being equal to or larger than that of said first exposed region.

36. The semiconductor device according to Claim 29, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

37. A semiconductor device comprising:

a semiconductor substrate having a first region of a first impurity concentration, first "second region", second "second region" and third "second region" each having a second impurity concentration being higher than that of said first region, and a third region having an impurity concentration being higher than said first impurity concentration and being lower than said second impurity concentration;

silicide layers each being formed in a manner so as to be in contact with a surface of each of said first "second region", second "second region" and third "second region";

one of a source electrode and a drain electrode being formed on one of the silicide layers formed in a manner so as to be in contact with the surface of said first "second region";

a gate electrode constructed between said silicide layers formed in a manner so as to be in contact with the surfaces of said first "second region" and second "second region"; and

another of said source electrode and said drain electrode being formed on another out of said silicide layers formed in a manner so as to be in contact with the surface of said third "second region";

wherein said first region is made up of a well region;

wherein said third region is formed on said first region;

wherein said third region makes up a first exposed region being exposed on a surface of said semiconductor substrate between said second "second region" and said third "second regions" and, on a surface of said semiconductor substrate, said third region and said second region are overlapped each other;

wherein each of said silicide layers is formed so as to have

a second exposed region in a manner that said second "second region" and third "second region" are in contact with said first exposed region in a continuous manner;

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second "second region" and third "second region"makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said first region makes up a high resistance region having a relatively high resistance value.

38. The semiconductor device according to Claim 37, wherein a field oxide film is formed on said first surface region or said first exposed region.

39. The semiconductor device according to Claim 37, wherein a gate electrode structure is formed on said first surface region or said first exposed region.

40. The semiconductor device according to Claim 37, wherein said second exposed region has a surface length being equal to or larger than that of said first exposed region.

41. The semiconductor device according to Claim 37, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

42. A method for manufacturing a semiconductor device comprising:

a step of implanting an impurity into a semiconductor substrate to form a first region of a first impurity concentration;

a step of forming first "second region", second "second region" and third "second region" each having an impurity concentration being higher than said first impurity concentration on said semiconductor substrate and of forming said second "second region" and third "second region" on both sides of said first region on a surface of said semiconductor substrate;

a step of forming silicide layers formed in a manner to be in contact with a surface of each of said first "second region", second "second region" and third "second region" in a manner that said first region has a first surface region not covered with said silicide layers and said second "second region" and third "second region" have second surface regions not covered with said silicide layers and said first surface region is sandwiched by two said second surface regions;

a step of forming a gate electrode constructed between said silicide layers formed in a manner so as to be in contact with the surfaces of said first "second region" and second "second region";

a step of forming one of a source electrode and a drain electrode being formed on the silicide layer formed in a manner so as to be in contact with the surface of said first "second region" and another of said source electrode and said drain electrode being formed on said silicide layer formed in a manner so as to be in contact with the surface of said third "second region";

wherein each of said silicide layers makes up a low

resistance region having a relatively low resistance value, each of said second surface regions makes up an intermediate resistance region having an intermediate resistance value, and said first surface region makes up a high resistance region having a relatively high resistance value.

43. The method for manufacturing a semiconductor device according to Claim 42, further comprising a step of forming a field oxide film formed on said first surface region or said first exposed region.

44. The method for manufacturing a semiconductor device according to Claim 42, further comprising a step of forming a gate electrode structure on said first surface region or on said first exposed region.

45. A method for manufacturing a semiconductor device comprising:

a step of implanting an impurity into a semiconductor substrate to form a first region of a first impurity concentration;

a step of forming first "second region", second "second region" and third "second region" each having an impurity concentration being higher than said first impurity concentration on said semiconductor substrate and said second "second region" and third "second region" are formed on a surface of said semiconductor substrate on both sides of said first exposed region so that said first region has a first exposed region being exposed on a surface of said semiconductor substrate;

a step of forming each of said silicide layers being in contact with a surface of each of said first "second region", second "second region" and third "second region" so that said second "second region" and third "second region" so as to have a second exposed region being successively in contact with said first exposed region of said first region;

a step of forming a gate electrode constructed between said silicide layers formed in a manner so as to be in contact with surfaces of said first "second region" and second "second region";

a step of forming one of a source electrode and a drain electrode being formed on the silicide layer formed in a manner so as to be in contact with a surface of said first "second region" and another of said source electrode and said drain electrode being formed on said silicide layer formed in a manner so as to be in contact with the surface of said third "second region";

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second region makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said first region makes up a high resistance region having a relatively high resistance value.

46. The method for manufacturing a semiconductor device according to Claim 45, wherein said second region are formed on a surface of said semiconductor substrate in a manner that said second region and said first region are overlapped.

47. The method for manufacturing a semiconductor device

according to Claim 46, wherein, said first impurity concentration of said first region, when it is assumed that a well region is formed on said semiconductor substrate, is higher than that of said well region.

48. The method for manufacturing a semiconductor device according to Claim 45, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

49. The method for manufacturing a semiconductor device according to Claim 45, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

50. The method for manufacturing a semiconductor device according to Claim 45, further comprising a step of forming a field oxide film formed on said first surface region or said first exposed region.

51. The method for manufacturing a semiconductor device according to Claim 45, further comprising a step of forming a gate electrode structure on said first surface region or on said first exposed region.

52. A method for manufacturing a semiconductor device comprising:

a step of implanting an impurity into a semiconductor substrate to form a first region of a first impurity

concentration;

a step of forming a third region having a thirs impurity concentration being higher than said first impurity concentration in a manner that said third region and said first region are overlapped on a surface of said semiconductor substrate;

a step of forming first "second region", second "second region" and third "second region" each having a second impurity concentration being higher than said third impurity concentration in said third region on said semiconductor substrate and said second "second region" and third "second region" are formed on a surface of said semiconductor substrate on both sides of said first exposed region so that said third region has a first exposed region being exposed on a surface of said semiconductor substrate;

a step of forming each of said silicide layers being in contact with a surface of each of said first "second region", second "second region" and third "second region" so that said second "second region" and third "second region" are exposed successively so as to be in contact with said first exposed region of said first region;

a step of forming a gate electrode constructed between said silicide layers formed in a manner so as to be in contact with the surfaces of said first "second region" and second "second region";

a step of forming one of a source electrode and a drain electrode being formed on one of the silicide layers formed in a manner so as to be in contact with the surface of said first "second region" and another of said source electrode and said drain electrode being formed on another out of said silicide layers formed in a manner so as to be in contact with the surface

of said third "second region";

wherein each of said silicide layers makes up a low resistance region having a relatively low resistance value, each of said second exposed regions in said second region makes up an intermediate resistance region having an intermediate resistance value, and said first exposed region in said third region makes up a high resistance region having a relatively high resistance value.

53. The method for manufacturing a semiconductor device according to Claim 52, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

54. The method for manufacturing a semiconductor device according to Claim 52, wherein a surface length of said second exposed region is equal to or larger than a depth of said second region.

55. The method for manufacturing a semiconductor device according to Claim 52, further comprising a step of forming a field oxide film formed on said first surface region or said first exposed region.

56. The method for manufacturing a semiconductor device according to Claim 52, further comprising a step of forming a gate electrode structure on said first surface region or on said first exposed region.